WHAT IS CLAIMED IS:

1. An impulsive type liquid crystal driving device, comprising:

a liquid crystal panel for including a plurality of gate bus lines, which are arranged in one-direction, and a plurality of data bus lines which are arranged in a direction perpendicular to the plurality of gate bus lines;

a gate driver section for sequentially scanning the plurality of gate bus lines during an active address interval in response to a second vertical starting signal, a vertical clock signal and an output enable signal, and scanning the plurality of gate bus lines during a vertical blanking interval in a unit of a predetermined number of lines; and

a current boosting section for increasing current amount supplied to the gate bus lines during the vertical blanking interval in response to a pulse width modulation signal.

2. The liquid crystal driving device according to claim 1, wherein, when a refresh rate is 60Hz, the active address interval is driven at 85Hz.

3. The liquid crystal driving device according to claim 1, wherein the gate driver section includes a plurality of

gate driver integrated circuits for scanning the plurality of gate bus lines in response to the second vertical starting signal, the vertical clock signal and the output enable signal.

4. The liquid crystal driving device according to claim 3, wherein each of the gate driver integrated circuit includes:

a first shift register section which outputs the second vertical starting signal after sequentially shifting it, during the active address interval, and generates a predetermined number of first output signals at the same time after receiving the second vertical starting signal during the vertical blanking interval, in response to the vertical clock signal and the output enable signal;

a second shift register section which receives the signal shifted by the first shift register section and then outputs it after sequentially shifting it, during the active address interval, and generates a predetermined number of second output signals at the same time after receiving the signal shifted by the first shift register section during the vertical blanking interval, in response to the vertical clock signal;

a plurality of level shifters which level-convert the

output signals of the first and the second shift register section; and

a plurality of buffer amplifiers which amplify the signals converted by the plurality of level shifters and then generates gate on/off signals.

5. The liquid crystal driving device according to claim 4, wherein the first shift register section includes:

a predetermined number of first switches which select either the second vertical starting signal or an internally shifted signal in response to the output enable signal; and

a predetermined number of first shift registers which receive the second vertical starting signal and then output it after sequentially shifting it, when the internally shifted signal is selected, and which receive the second vertical starting signal and then output the predetermined number of first output signals at the same time without shifting, when the second vertical starting signal is selected.

6. The liquid crystal driving device according to claim 4, wherein the second shift register section includes:

a plurality of second switches which select either the signal shifted by the first shift register section or an

internally shifted signal in response to the output enable signal; and

a predetermined number of second shift registers which receive the second vertical starting signal and then output it after sequentially shifting it, when the internally shifted signal is selected, and which receive the shifted signal and then output the predetermined number of second output signals at the same time without shifting, when the signal shifted by the first shift register section is selected.

7. The liquid crystal driving device according to claim 1, wherein the current boosting section includes a plurality of current booster circuits for receiving a plurality of gate on/off signals outputted from the gate driver section and a pulse width modulation signal, respectively.

8. The liquid crystal driving device according to claim 7, wherein the current booster circuit includes:

an operational amplifier having a non-inverting terminal and an inverting terminal;

a first resistor coupled between the non-inverting terminal and a ground;

a first capacitor coupled in parallel to the first

resistor;

a second capacitor coupled between a first input terminal and the ground;

a second resistor of which one end is coupled to the first input terminal;

a first bipolar transistor coupled between the other end of the second resistor and a ground, and turned on according to an output signal of the operational amplifier;

a third resistor of which one end is coupled to the first input terminal;

a second bipolar transistor coupled between other end of the third resistor and the non-inverting terminal, and turned on according to an output signal of other end of the second resistor;

a fourth resistor coupled between the first input terminal and the non-inverting terminal;

a third capacitor coupled between the inverting terminal of the operational amplifier and an output terminal;

a fifth resistor coupled between a second input terminal and the inverting terminal;

a sixth resistor coupled between the inverting terminal and a ground; and

a fourth capacitor coupled in parallel to the sixth resistor.

9. The liquid crystal driving device according to claim 8, wherein the first and the second first bipolar transistor are p-type transistors.

10. The liquid crystal driving device according to claim 1, wherein the current amount generated in the current boosting section is adjusted according to a duty ratio of the pulse width modulation signal.